ABSTRACT OF THE DISCLOSURE

A memory transistor of an EEPROM has a floating gate electrode of a shape such that it covers the entirety of a tunnel film and a channel region and does not cover a region between the channel region and an embedded layer. And, a control gate electrode is formed on an interlayer insulating film on the floating gate electrode into a shape such that it is wider than the floating gate electrode above the tunnel film, and is narrower than the floating gate electrode above the channel region.